What is claimed is:

1. A method of a network processor comprising a plurality of microengines that process network packets, the method comprising

updating an entry in a memory external to the network processor;

identifying a microengine of the plurality of microengines that has stored the entry in a local memory for the microengine; and

writing information to a buffer for the identified microengine that indicates the entry has been updated.

2. The method of claim 1 further comprising updating the entry in the local memory for the microengine in response to determining, based upon the information written to the buffer, that the entry has been updated.

3. The method of claim 1 further comprising

reading the entry from the memory external to the network processor in response to determining, based upon the information written to the buffer, that the entry has been updated; and

updating the local memory for the microengine based upon the entry read from the memory external to the network processor.

4. The method of claim 1 further comprising

updating the entry in the local memory for the microengine in response to determining, based upon the information written to the buffer, that the entry has been updated; and

processing a network packet based upon the entry updated in the local memory for the microengine.

5. The method of claim 1 further comprising designating at least one thread of each microengine of the plurality of microengines to update entries of a corresponding local memory for each microengine based upon information stored in a corresponding buffer for each microengine.

6. The method of claim 1 further comprising activating a thread of the microengine to process information stored in the buffer and to update the local memory of the microengine based upon the information stored in the buffer.

7. The method of claim 1 further comprising determining that all entries in the local memory for the microengine are invalid based upon the information stored in the buffer for the microengine.

8. The method of claim 1 further comprising determining that all entries in the local memory for the microengine are outdated based upon the information stored in the buffer for the microengine.

9. A network processor to process network packets based upon entries stored in an external memory, comprising:

a plurality of microengines to process network packets, each microengine having a corresponding local memory to cache entries stored in the external memory and a corresponding buffer to identify entries in the local memory updated in the external memory, and

a control plane to update an entry in the external memory, to identify each microengine of the plurality of microengines having the entry stored in the corresponding local memory, and to store an identifier for the entry in the corresponding buffer for each identified microengine to indicate that the entry has been updated in the external memory.

10. The network processor of claim 9 wherein the control plane comprises at least one processing core to update the entry, to identify each microengine, and to store the identifier in the corresponding buffer for each identified microengine.

11. The network processor of claim 9 wherein each microengine

reads the entry from the external memory in response to determining, based upon the identifier written to the corresponding buffer, that the entry has been updated, and

updates the corresponding local memory based upon the entry read from the external memory.

12. The network processor of claim 9 wherein each microengine

updates the entry in the corresponding local memory in response to determining, based upon the identifier written to the corresponding buffer, that the entry has been updated, and

processes a network packet based upon the entry updated in the corresponding local memory.

13. The network processor of claim 9 wherein each microengine comprises a plurality of threads to process network packets and at least one thread to update entries of the corresponding local memory upon identifiers for entries stored in the corresponding buffer.

14. A network device, comprising:

a plurality of ports to transfer network packets;

a memory to store entries used to process network packets;

a network processor to process network packets based upon the entries stored in the memory external to the network processor, wherein the network processor comprises

a plurality of microengines to process network packets, each microengine having a corresponding local memory to cache entries stored in the external memory and a corresponding buffer to identify entries in the local memory updated in the external memory, and

at least one processing core to control the plurality of microengines, to update entries in the memory external to the network processor, to identify each microengine of the plurality of microengines having updated entries of the memory stored in corresponding local memory, and to store information in the corresponding buffer for each identified microengine to indicate updated entries of the memory.

15. The network device of claim 14 wherein each microengine

reads updated entries from the memory based upon the information in the corresponding buffer, and

updates the corresponding local memory based upon the updated entries read from the memory.

16. The network device of claim 14 wherein each microengine

updates entries in the corresponding local memory based upon information in their corresponding buffer, and

processes network packets based upon the entries updated in the corresponding local memory.

17. The network device of claim 14 wherein each microengine comprises a plurality of threads to process network packets, wherein at least one thread of the plurality of threads updates entries of the corresponding local memory based upon information in the corresponding buffer.

18. The network device of claim 14 wherein

each microengine comprises a plurality of threads to process network packets, and

the at least one processing core designates at least one thread of each microengine to update entries of the corresponding local memory of the microengine based upon information in the corresponding buffer of the microengine.

19. A machine readable medium comprising a plurality of instructions that in response to being executed result in a network device

updating an entry in a memory external to a network processor of the network device;

identifying each microengine of the network processor that has cached the entry in a local memory of the network processor;

storing information to a corresponding buffer for each identified microengine, the information indicating the entry has been updated in the memory external to the network processor; and

updating the entry cached in the local memory based upon the information in the corresponding buffer for each identified microengine.

20. The machine readable medium of claim 19 wherein the plurality of instructions further result in the network device

reading the entry from the memory external to the network processor in response to determining, based upon the information written to the buffer, that the entry has been updated; and

updating the entry cached in the local memory based upon the entry read from the memory external to the network processor.

21. The machine readable medium of claim 19 wherein the plurality of instructions further result in the network device processing a network packet based upon the updated entry cached in the local memory.

22. The machine readable medium of claim 19 wherein the plurality of instructions further result in the network device designating at least one thread of each microengine of the plurality of microengines to update entries of the local memory based upon information stored in the corresponding buffer for each microengine.